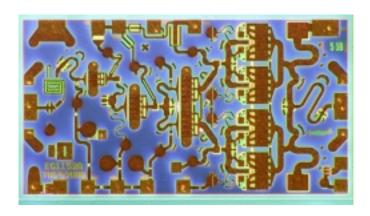
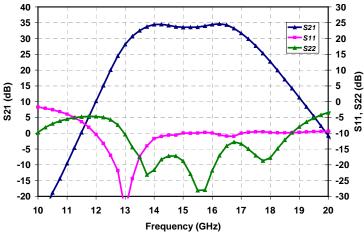


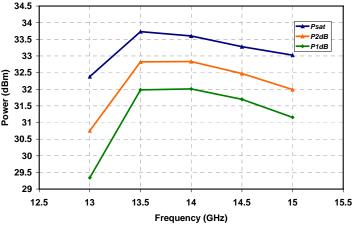
13.5 - 15 GHz 2 Watt Power Amplifier

TGA1152-EPU



Preliminary Measured Performance





Key Features

- 0.5 um pHEMT Technology
- 34 dB Nominal Gain
- 31.7dBm Nominal Pout @ P1dB
- >2W Psat at 14.5GHz
- OTOI 39dBm Typical
- Bias 7V @ 680 mA
- Chip Dimensions 1.390mm x 2.495mm

Primary Applications

- Ku Band Sat-Com
- Point-to-Point Radio

Samples Available Q201 Measured Performance Summary

<u>PARAMETER</u>	<u>UNITS</u>	TYPICAL
FREQUENCY	GHz	13.5-15
SMALL SIGNAL GAIN	dB	34
NOISE FIGURE	dB	N/A
INPUT RETURN LOSS	dB	-10
OUTPUT RETURN LOSS	dB	-17
P1db @ 14.5 GHz	dBm	32 (25C)
GAIN FLATNESS 14-14.5 GHz	dB	+/- 0.25
GAIN FLATNESS 13.5-14.5 GHz	dB	+/- 1.0
IMP3@SCL = P1dB - 10dB	dBc	35
OIP3 (P1dB-10dB)	dBc	39
V_{dd}	V	7
NOMINAL SMALL SIGNAL BIAS CURRENT	mA	680
BIAS CURRENT AT P1dB	mA	870
SIZE	mm ²	3.46

Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice



Advance Product Information TGA1152-EPU

TABLE I MAXIMUM RATINGS

SYMBOL	PARAMETER <u>5</u> /	VALUE	NOTES
V^+	POSITIVE SUPPLY VOLTAGE 8 V		
V ⁻	NEGATIVE SUPPLY VOLTAGE RANGE	-5V TO 0V	
I ⁺	POSITIVE SUPPLY CURRENT (QUIESCENT)	1.023 A	<u>4/</u>
$ I_G $	GATE SUPPLY CURRENT	35.2 mA	
P_{IN}	INPUT CONTINUOUS WAVE POWER	21.4 dBm	
P_{D}	POWER DISSIPATION	9.404 W	<u>3</u> / <u>4/</u>
T _{CH}	OPERATING CHANNEL TEMPERATURE	150 °C	<u>1</u> / <u>2</u> /
T_{M}	MOUNTING TEMPERATURE (30 SECONDS)	320 °C	
T _{STG}	STORAGE TEMPERATURE	-65 to 150 ⁰ C	

- $\underline{1}$ / These ratings apply to each individual FET.
- $\underline{2}$ / Junction operating temperature will directly affect the device median time to failure (T_M). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.
- 3/ When operated at this bias condition with a base plate temperature of 70 °C, the median life is reduced from 8.9E+6 to 4.2 E+4 hours.
- $\underline{4}$ / Combinations of supply voltage, supply current, input power, and output power shall not exceed P_D .
- 5/ These ratings represent the maximum operable values for this device.



TGA1152-EPU

DC SPECIFICATIONS (100%) $(T_A = 25 \text{ °C} \pm 5 \text{ °C})$

NOTES	SYMBOL	TEST CONDITIONS <u>2</u> /	LIMITS		UNITS
			MIN	MAX	
	I_{DSS}	STD	Info only	200	mA
	Gm	STD	Info only	252	mS
<u>1</u> /	$ V_{P1} $	STD	0.5	1.5	V
<u>1</u> /	$ V_{P2} $	STD	0.5	1.5	V
1/	$ V_{P3} $	STD	0.5	1.5	V
<u>1</u> /	$ V_{\mathrm{BVGD}} $	STD	13	30	V
<u>1</u> /	$ V_{\mathrm{BVGS}} $	STD	13	30	V

- $\underline{1}/$ V_P , V_{BVGD} , and V_{BVGS} are negative.
- 2/ The measurement conditions are subject to change at the manufacture's discretion

PRELIMINARY RF SPECIFICATIONS

$$(T_A = 25^{\circ}C \pm 5^{\circ}C)$$

NOTE	TEST	MEASUREMENT CONDITIONS 7V @ 682mA +/- 5%	VALUE			UNITS
			MIN	TYP	MAX	
	SMALL-SIGNAL GAIN MAGNITUDE	13.5 – 16.5 GHz		34		dB
	POWER OUTPUT AT Pin = +3 dBm	14.5 GHz	31			dBm
	PAE at Pin = $+3$ dBm	14.5 GHz	23			%
	INPUT RETURN LOSS MAGNITUDE	13.5 – 16.5 GHz		-10		dB
	OUTPUT RETURN LOSS MAGNITUDE	13.5 – 16.5 GHz		-10		dB

Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice



TGA1152-EPU

THERMAL INFORMATION*

Parameter	Test Conditions	T _{CH} (°C)	R _{0JC} (°C/W)	T _M (HRS)
$R_{\theta JC}$ Thermal Resistance (channel to backside of carrier)	Vd = 7V $I_D = 682 \text{ mA}$ Pdiss = 4.774 W	125.74	11.67	8.9E+6

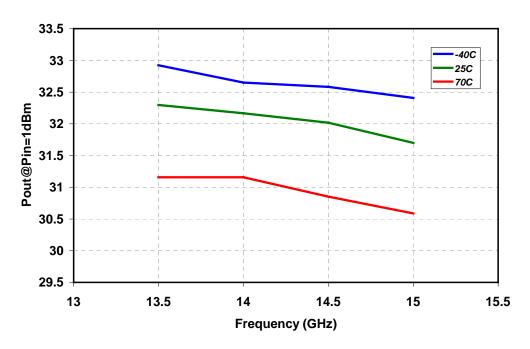
Note: Assumes eutectic attach using 1.5 mil 80/20 AuSn mounted to a 20 mil CuMo Carrier at 70°C baseplate temperature. Worst case condition with no RF applied, 100% of DC power is dissipated.

^{*} The thermal information is a result of a detailed thermal model.

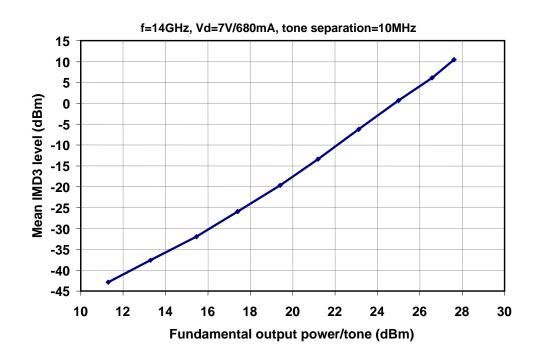


TGA1152-EPU

TGA1152 Over Temperature Measured Performance 6V @ 680mA

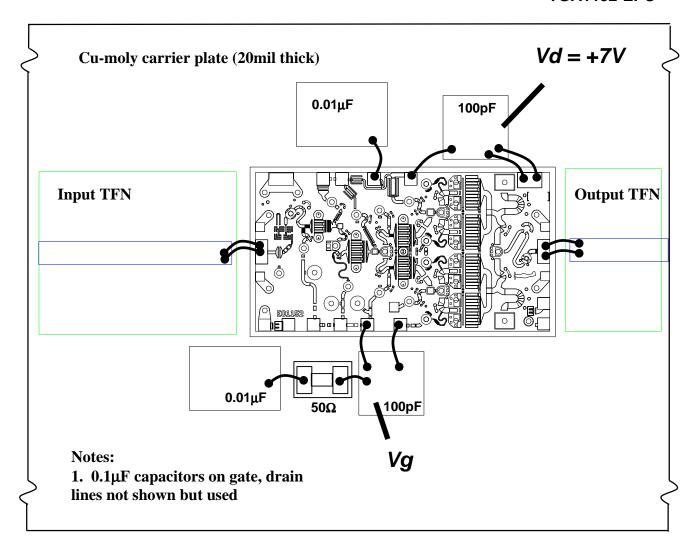


TGA1152 IMD3 Performance





TGA1152-EPU



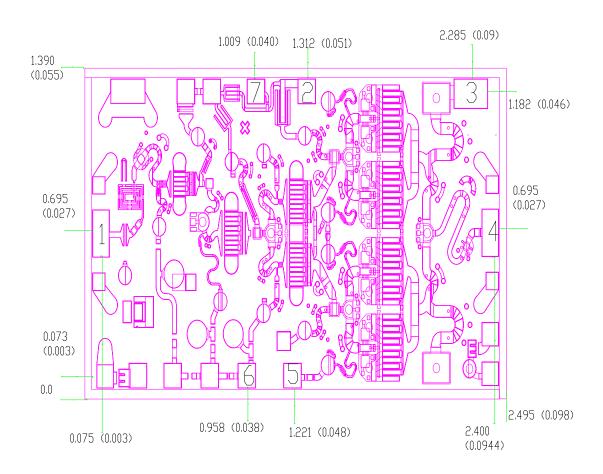
Recommended Assembly Diagram

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice



Advance Product Information TGA1152-EPU



Units: millimeters (inches) Thickness: 0.1016 (0.004)

Chip edge to bond pad dimensions are shown to center of bond pad

Chip size tolerance: +/- 0.051 (0.002)

 Bond pad #1 (RF Input)
 0.100 x 0.200 (0.004 x 0.008)

 Bond pad #2 (Vd)
 0.100 x 0.100 (0.004 x 0.004)

 Bond pad #3 (Vd)
 0.125 x 0.200 (0.005 x 0.008)

 Bond pad #4 (RF Dutput)
 0.100 x 0.200 (0.004 x 0.008)

 Bond pad #5, #6 (Vg)
 0.100 x 0.100 (0.004 x 0.004)

 Bond pad #7 (Bypass)
 0.100 x 0.100 (0.004 x 0.004)



TGA1152-EPU

Reflow process assembly notes:

- AuSn (80/20) solder with limited exposure to temperatures at or above 300°C
- alloy station or conveyor furnace with reducing atmosphere
- no fluxes should be utilized
- coefficient of thermal expansion matching is critical for long-term reliability
- storage in dry nitrogen atmosphere

Component placement and adhesive attachment assembly notes:

- vacuum pencils and/or vacuum collets preferred method of pick up
- avoidance of air bridges during placement
- force impact critical during auto placement
- organic attachment can be used in low-power applications
- curing should be done in a convection oven; proper exhaust is a safety concern
- microwave or radiant curing should not be used because of differential heating
- coefficient of thermal expansion matching is critical

Interconnect process assembly notes:

- thermosonic ball bonding is the preferred interconnect technique
- force, time, and ultrasonics are critical parameters
- aluminum wire should not be used
- discrete FET devices with small pad sizes should be bonded with 0.0007-inch wire
- maximum stage temperature: 200°C

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.